REMARKS

In the non-final Office Action, the Examiner rejected claims 39, 41, 45-50, 53, 54, 57-60, 63-66, and 71 under 35 U.S.C. § 102(b) as anticipated by Munter et al. (U.S. Patent No. 5,126,999); and rejected claims 42-44, 51, 52, 55, 56, 61, 62, 69, 70, and 72 under 35 U.S.C. § 103(a) as unpatentable over Munter et al. in view of Suzuki (U.S. Patent No. 4,799,215).

By this Amendment, Applicants amend claim 49 to improve form. Applicants respectfully traverse the Examiner's rejections under 35 U.S.C. §§ 102 and 103. Claims 39-72 remain pending.

Initially, Applicants note that the Examiner did not reject claims 40, 67, and 68, but also did not identify these claims as allowable. Applicants assume that the Examiner meant to identify these claims as allowable. Nevertheless, Applicants respectfully request clarification as to the status of these claims.

In paragraph 2 of the Office Action, the Examiner rejected claims 39, 41, 45-50, 53, 54, 57-60, 63-66, and 71 as allegedly anticipated by Munter et al. Applicants respectfully traverse the rejection.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. In other words, the identical invention must be shown in as complete detail as contained in the claim. See M.P.E.P. § 2131. Munter et al. does not disclose or suggest the combination of features recited in claims 39, 41, 45-50, 53, 54, 57-60, 63-66, and 71.

Claim 39, for example, is directed to an apparatus for processing packets. The apparatus comprises a first input queue configured to receive a stream of incoming packets and to output

beginning portions of packets as the beginning portions are received without waiting for the respective packets to be received in their entirety; a first in-line packet processor for receiving the beginning portions from the first input queue, each beginning portion including first header information, and for detecting the existence of an error in the first header information of each beginning portion; and a first memory for storing packets received at the first input queue and for which the first in-line packet processor did not detect an error in the corresponding first header information.

Munter et al. does not disclose or suggest the combination of features recited in claim 39. For example, Munter et al. does not disclose or suggest a first input queue configured to receive a stream of incoming packets and to output beginning portions of packets as the beginning portions are received without waiting for the respective packets to be received in their entirety.

The Examiner alleged that item 31A in Munter et al. corresponds to the first input queue recited in claim 39 (Office Action, page 2). Applicants respectfully disagree.

Munter et al. describes item 31A as an input buffer (Fig. 3). Munter et al. describes the operation of th input buffer as:

> We now turn to FIG. 4 of the drawings, which is a block schematic showing an input buffer 40, being a random-access-memory (RAM) organized into 16 independent FIFOs each of which is 128 packets long; each packet is 80 Bytes in length. The high speed input data stream is demultiplexed from 6 to 12 bit code and, after elastic buffering, enters a header address modifier prior to entering the buffer 40, where the packets are stored in FIFOs F1 to F16 depending on each packets's switch output port destination. This is accomplished by decoding each packet header in header decoder 41, the output of which steers the packets into the appropriate FIFO F1 to F16 via input buffer interface 42. The data are stored in the FIFOs in 12 bit 10B12B code words. As a data packet is being written into a FIFO, an error detector 43 is calculating its own check byte for the entire packet. As the packet ends, the locally calculated check byte is compared to the one received from the header and the faulty packet is discarded upon non-coincidence and the FIFO's write pointer is reset to the last byte of the previous packet address. If there is coincidence and the pockets is not faulty, the number of packets in that FIFO is incremented accordingly and the buffer fill information is output on the FILL bus.

(col. 5, line 54 - col. 6, line 9). In this section, Munter et al. discloses that as packet data is received in the input data stream, it is demultiplexed, elastic buffered, and stored in a FIFO based on the packet's switch output port destination. Munter et al. discloses that the packet's header is decoded by a header decoder prior to the packet being stored in a FIFO to determine the packet's switch output port destination. Munter et al. also discloses that as a packet is being written into a FIFO, an error detector calculates a check byte for the entire packet.

Nowhere in this section, or elsewhere, does Munter et al. disclose or suggest a first input queue that is configured to receive a stream of incoming packets and to output beginning portions of packets as the beginning portions are received without waiting for the respective packets to be received in their entirety, as required by claim 39. In other words, nowhere does Munter et al. disclose or suggest that beginning portions of packets are output to the header decoder or the error detector (which the Examiner alleged were the equivalent of the first in-line packet processor recited in claim 39) as the beginning portions are received without waiting for the respective packets to be received in their entirety. Any allegation to the contrary is based solely on speculation without any support in the disclosure of Munter et al.

For at least these reasons, Applicants submit that claim 39 is not anticipated by Munter et al. Claims 41 and 45-48 depend from claim 39 and are, therefore, not anticipated by Munter et al. for at least the reasons given with regard to claim 39. Claims 41 and 45-58 are also not anticipated by Munter et al. for reasons of their own.

For example, claim 41 recites that the first in-line packet processor generates a signal to drop a packet before the packet is stored in the first memory and for which it detects an error in the corresponding first header information. Munter et al. does not disclose or suggest the

combination of features recited in claim 41.

The Examiner identified item 41 (header decoder) and item 43 (error detector) of Munter et al. as allegedly corresponding to the first in-line packet processor and item 40 (buffer) of Munter et al. as allegedly corresponding to the first memory (Office Action, page 2). Even assuming, for the sake of argument, that header decoder 41 and error detector 43 could be equated to the first in-line packet processor and buffer 40 can be equated to the first memory (points that Applicants do not concede), nowhere does Munter et al. disclose or suggest that either header decoder 41 or error detector 43 generates a signal to drop a packet before the packet is stored in buffer 40 and for which it detects an error in the corresponding first header information, as would be required by claim 41.

In fact, Munter et al. specifically teaches against the features of claim 41. Munter et al. discloses:

> As a data packet is being written into a FIFO, an error detector 43 is calculating its own check byte for the entire packet. As the packet ends, the locally calculated check byte is compared to the one received from the header and the faulty packet is discarded upon non-coincidence and the FIFO's write pointer is reset to the last byte of the previous packet address.

(col. 5, line 67 - col. 6, line 6). In this section, Munter et al. discloses that the packet is written into the FIFO (of buffer 40) and if the locally calculated check byte does not match the one in the header of the packet, then the packet is discarded from the FIFO. This is directly contrary to generating a signal to drop a packet before the packet is stored in buffer 40 and for which it detects an error in the corresponding first header information, as would be required by claim 41.

For at least these additional reasons, Applicants submit that claim 41 is not anticipated by Munter et al.

Independent claim 49 is directed to a device for processing packets. The device comprises an input queue for receiving a stream of packets and for outputting beginning portions of packets as the beginning portions are received without waiting for the respective packets to be received in their entirety; and a header processor configured to receive the beginning portions from the input queue, each beginning portion including first header information, for detecting the existence of an error in the first header information included in each beginning portion. Upon detecting the existence of an error in a first header information, the header processor generates an error signal indicating that the corresponding packet contains an error.

Munter et al. does not disclose or suggest the combination of features recited in claim 49. For example, Munter et al. does not disclose or suggest an input queue for receiving a stream of packets and for outputting beginning portions of packets as the beginning portions are received without waiting for the respective packets to be received in their entirety.

The Examiner alleged that item 31A in Munter et al. corresponds to the input queue recited in claim 49 (Office Action, page 2). Applicants respectfully disagree for at least reasons similar to the reasons given with regard to claim 39.

For at least these reasons, Applicants submit that claim 49 is not anticipated by Munter et al. Claim 50 depends from claim 49 and is, therefore, not anticipated by Munter et al. for at least the reasons given with regard to claim 49. Claim 50 is further not anticipated by Munter et al. for reasons of its own.

Claim 50 recites a buffer manager for causing each packet received at the input queue to be stored in memory if the buffer manager does not receive an error signal corresponding to the packet from the header processor. Munter et al. does not disclose or suggest the combination of

features recited in claim 50. The Examiner did not address the features of claim 50 and, therefore, did not establish a proper case of anticipation with regard to claim 50.

For at least these additional reasons, Applicants submit that claim 50 is not anticipated by Munter et al.

Independent claim 53 is directed to a device for packet processing. The device comprises an input queue for sequentially receiving portions of a packet, a first portion including a first packet header, and for outputting the first portion before the remaining portions are received; a header processor, coupled to the input queue, configured to process the first packet header included in the first portion prior to transferring any portions of the packet into a packet memory; and a buffer manager, coupled to the input queue and the header processor, configured to cause the portions of the packet received at the input queue to be stored in the packet memory if no signal is received from the header processor to drop the packet.

Munter et al. does not disclose or suggest the combination of features recited in claim 53. For example, Munter et al. does not disclose or suggest an input queue for sequentially receiving portions of a packet, a first portion including a first packet header, and for outputting the first portion before the remaining portions are received.

The Examiner alleged that item 31A in Munter et al. corresponds to the input queue recited in claim 53 (Office Action, page 2). Applicants respectfully disagree for at least reasons similar to the reasons given with regard to claim 39.

Munter et al. also does not disclose or suggest a buffer manager, coupled to the input queue and the header processor, configured to cause the portions of the packet received at the input queue to be stored in the packet memory if no signal is received from the header processor

to drop the packet, as recited in claim 53. The Examiner did not address these features and, therefore, did not establish a proper case of anticipation with regard to claim 53.

For at least these reasons, Applicants submit that claim 53 is not anticipated by Munter et al. Claims 54, 57, and 58 depend from claim 53 and are, therefore, not anticipated by Munter et al. for at least the reasons given with regard to claim 53.

Independent claim 59 is directed to a device for packet processing. The device comprises an input queue for sequentially receiving portions of a packet, a first portion including a first packet header for the packet, and for outputting the first portion before the remaining portions are received; a header processor, coupled to the input queue, configured to process the first packet header included in the first portion prior to transferring any portions of the packet into a packet memory; and a buffer manager, coupled to the input queue and the header processor, configured to cause the portions of the packet received at the input queue to be stored in the packet memory after receiving a signal from the header processor indicating acceptance of the packet.

Munter et al. does not disclose or suggest the combination of features recited in claim 59. For example, Munter et al. does not disclose or suggest an input queue for sequentially receiving portions of a packet, a first portion including a first packet header for the packet, and for outputting the first portion before the remaining portions are received.

The Examiner alleged that item 31A in Munter et al. corresponds to the input queue recited in claim 59 (Office Action, page 2). Applicants respectfully disagree for at least reasons similar to the reasons given with regard to claim 39.

Munter et al. also does not disclose or suggest a buffer manager, coupled to the input

queue and the header processor, configured to cause the portions of the packet received at the input queue to be stored in the packet memory after receiving a signal from the header processor indicating acceptance of the packet, as recited in claim 59. The Examiner did not address these features and, therefore, did not establish a proper case of anticipation with regard to claim 59.

For at least these reasons, Applicants submit that claim 59 is not anticipated by Munter et al. Claims 60, 63, and 64 depend from claim 59 and are, therefore, not anticipated by Munter et al. for at least the reasons given with regard to claim 59.

Independent claim 65 is directed to a method of processing a packet. The method comprises receiving portions of a packet in a stream; forming a beginning portion of the packet as the portions are received without waiting for the entire packet to be received, the beginning portion containing first header information; while the remaining portions of the packet are being received, detecting the existence of an error in the beginning portion; and dropping the packet upon existence of an error in the packet.

Munter et al. does not disclose or suggest the combination of features recited in claim 65. For example, Munter et al. does not disclose or suggest forming a beginning portion of the packet as the portions are received without waiting for the entire packet to be received, where the beginning portion contains first header information. The Examiner did not address this feature. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 65.

Munter et al. also does not disclose or suggest detecting the existence of an error in the beginning portion while the remaining portions of the packet are being received, as further recited in claim 65. Instead, Munter et al. clearly discloses detecting a faulty packet after the packet is stored in the FIFO (col. 5, line 67 - col. 6, line 6). The Examiner also did not address

this feature. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 65.

For at least these reasons, Applicants submit that claim 65 is not anticipated by Munter et al. Claims 66 and 71 depend from claim 65 and are, therefore, not anticipated by Munter et al. for at least the reasons given with regard to claim 65.

For at least the foregoing reasons, Applicants respectfully request the reconsideration and withdrawal of the rejection of claims 39, 41, 45-50, 53, 54, 57-60, 63-66, and 71 under 35 U.S.C. § 102 based on Munter et al.

In paragraph 5 of the Office Action, the Examiner rejected claims 42-44, 51, 52, 55, 56, 61, 62, 69, 70, and 72 under 35 U.S.C. § 103(a) as allegedly unpatentable over Munter et al. in view of Suzuki. Applicants respectfully traverse the rejection.

Claims 42-44 and 72 depend from claim 39, claims 51 and 52 depend from claim 49, claims 55 and 56 depend from claim 53, claims 61 and 62 depend from claim 59, and claims 69 and 70 depend from claim 65. Without acquiescing in the Examiner's rejection, Applicants respectfully submit that the disclosure of Suzuki does not cure the deficiencies in the disclosure of Munter et al. identified above with regard to claims 39, 49, 53, 59, and 65. Therefore, claims 42-44, 51, 52, 55, 56, 61, 62, 69, 70, and 72 are patentable over Munter et al. and Suzuki, whether taken alone or in any reasonable combination, for at least the reasons given with regard to claims 39, 49, 53, 59, and 65.

For at least the foregoing reasons, Applicants respectfully request the reconsideration and withdrawal of the rejection of claims 42-44, 51, 52, 55, 56, 61, 62, 69, 70, and 72 under 35 U.S.C. § 103 based on Munter et al. and Suzuki.

If the Examiner does not believe that all pending claims are now in condition for allowance, the Examiner is urged to contact the undersigned to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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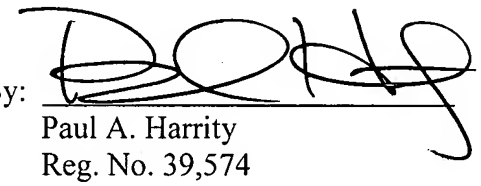
By: 
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Date: September 7, 2005

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